REMARKS

Claims 1-14, 16-20 and 23-25 are pending. Claims 1, 20 and 23 are amended herein. Reconsideration of the Application and Claims is respectfully requested.

102 Rejection

Claims 1-14, 16-20 and 23-25 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee et al. (US Patent Application No. 2003/0158995) in view of Chan et al. (US Patent No. 6,230,249). Applicant respectfully submits that Lee et al. in view of Chan et al. does not anticipate or render obvious the embodiments of the present invention as are set forth in Claims 1-14, 16-20 and 23-25.

The Examiner is respectfully directed to Claim 1, which is drawn to a variable width memory system. Claim 1 is reproduced below in its entirety for the Examiner's convenient reference.

> 1. A variable width memory system comprising:
> a bus for communicating information;
> a plurality of single cell variable width memory locations coupled to said bus, said plurality of single cell variable width memory locations store information, wherein said plurality of single cell variable width memory locations receive a number of bits corresponding to the width of the single cell variable width memory locations and the width of a variable width register that is located in a processor associated with the variable width memory system; and
> a controller coupled to said bus, said controller directs access to said plurality of single cell variable width memory locations, wherein said number of bits potentially vary automatically on a per access basis depending on which single cell variable width memory location of said plurality of single cell variable width memory locations is being accessed, wherein all memory locations are not required to have the same width.

Claims 8, 20 and 23 recite limitations that are similar to those contained in Claim 1. Claims 2-7 depend from independent Claim 1, Claims 9-14 and 16-19 depend from independent Claim 8 and Claims 24-25 depend from independent Claim 23 and set forth additional limitations of the present claimed invention.

Lee et al. does not anticipate or render obvious the embodiments of the present invention that are set forth in Claims 1, 8, 20 and 23. A shortcoming of the Lee et al. reference is that Lee et al. does not teach or suggest all of the limitations that are recited in the aforementioned Claims as is required to anticipate or render obvious the embodiments of the present invention set forth therein. In particular, Lee et al. does not teach or suggest a variable width memory system that includes "a plurality of single cell variable width memory locations" that "store information" and that "receive a number of bits corresponding to the width of the variable width memory locations and the width of a variable width register that is located in a processor associated with the variable width memory system" as is set forth in Claim 1 (Claims 8, 20 and 23 contain similar limitations).

Lee et al. only discloses a dissimilar method for DRAM control with adjustable page size. Lee discloses that as a part of the disclosed method for DRAM control, page size can be adjusted by using memory masks. It should be noted that Lee et al. discloses adjusting page size and is not concerned with adjusting the width of a particular memory location (e.g., a cell) as is required to meet the limitations of Applicant's Claim 1 (Claims 8, 20 and 23 contain similar limitations). In addition, it is important to note that Lee et al. does not associate a width of a variable width register that is located in a processor associated with the variable width memory system with the width of a single cell variable width memory location as is required to meet the limitations of Claim 1 (Claims 8, 20 and 23 contain similar limitations).

Furthermore, Applicant respectfully submits that nowhere in the Lee et al. reference is it taught or suggested that a variable width memory system include a plurality of single cell variable width memory locations that store information and that receive a number of bits corresponding to the width of the variable width memory locations and the width of a register that is located in the processor that is associated with the variable width memory as is set forth in Claim 1 (Claims 8, 20 and 23 contain similar limitations).

Chan et al. does not teach or suggest a modification of Lee et al. that would remedy the deficiencies of Lee et al. outlined above. In particular, Lee et al. does not teach or suggest a variable width memory system that includes "a plurality of single cell variable width memory locations" that "store information" and that "receive a number of bits corresponding to the width of the variable width memory locations and the width of a variable width register that is located in a processor associated with the variable width memory system" as is set forth in Claim 1 (Claims 8, 20 and 23 contain similar limitations). Chan et al. only discloses a dissimilar method and apparatus for providing logical cell available information in a memory. However, Nowhere in the Chan et al. reference is the number of bits that are received into a memory location associated with the width of a variable width register that is located in a processor associated with the variable width memory system or any register for that matter.

The Examiner contends in the Response to Arguments section of the outstanding Office Action that Chan et al. discloses "a variable size circuit 200 that defines the number of bytes ... per cell for an access operation to a cell (Col. 5, lines 2-18)." Moreover, the Examiner equates the variable size circuit 200 with the recited variable width register. However, nothing in the descriptions provided in the Chan et al. reference indicates that the variable size circuit of Chan et al. is a register at all. Furthermore, the variable size circuit is not located in a processor. As such, this element cannot reasonably be equated with the variable width register that is recited in Claim 1 (Claims 8, 20 and 23 contain similar limitations). If the Examiner wishes to maintain the instant rejection on the basis of relevant teachings provided by the Chan et al. reference, Applicant respectfully requests that the specific location in the Chan et al. reference where this information is taught or suggested be identified.

Consequently, the embodiments of present invention that are set forth in Claims 1, 8, 20 and 23 are not anticipated or rendered obvious by Lee et al. in view of Chan et al. Accordingly, Applicant respectfully submits that Lee et al. in view of Chan et al. does not anticipate or render obvious the embodiments of the present claimed invention as are recited

in Claims 2-7 which depend from Claim 1, Claims 9-14 and 16-19 which depend from Claim 8, and Claims 24-25 which depend from Claim 23. Consequently, the rejection of Claims 1-14, 16-20 and 23-25 under 35 U.S.C. 103(a) is improper and should be withdrawn.

Conclusion

In light of the above-listed amendments and remarks, Applicant respectfully requests allowance of the remaining Claims.

The Examiner is urged to contact Applicant's representative Bill O'Meara whose telephone number is (970) 898-7917 if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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